CLAIMS

What is claimed is:

1. A circuit comprising:

a multiplexer;

a space control register coupled to control the multiplexer;

a latch coupled to receive a signal from the multiplexer;

a control circuit coupled to control the latch, the control circuit to select one or more bits from a stream of bits output by the multiplexer;

2. The circuit of claim 1 wherein the multiplexer comprises a plurality of multiplexers.

3. The circuit of claim 2 wherein the plurality of multiplexers comprise first, second, third, fourth and fifth multiplexers.

4. The circuit of claim 3 wherein the first, second, third and fourth multiplexers are 8:1 multiplexers.

5. The circuit of claim 3 wherein the fifth multiplexer comprises a 6:1 multiplexer coupled to receive an output from the first multiplexer, an output from the second multiplexer, an output from the third multiplexer, an output from the fourth multiplexer, a logical "one", and a logical "zero".

6. The circuit of claim 1 wherein the space control register programmably stores a value indicating a selected bit from a plurality of bits.

7. The circuit of claim 1 wherein the control circuit comprises:

a time control register to store a value indicating a selected bit from a sequence of bits;

a counter to count bits in the sequence of bits from a predetermined bit;

a comparator coupled to the time control register and to the counter to generate a load signal when a value stored in the time control register and a value provided by the counter are equal, the load signal to cause the latch to load a value output by the multiplexer.

8. The circuit of claim 1 further comprising:

a second multiplexer coupled to receive a signal output by the latch and to receive a signal output by another circuit; and

a second control circuit to control the second multiplexer.

9. The circuit of claim 8 further comprising second latch coupled to receive a signal output by the second multiplexer.

10. The circuit of claim 1, wherein the multiplexer receives logical values to generate alarm signals.

11. A method comprising:

receiving multiple streams of bits; and

selecting one or more bits from a stream of bits based, at least in part, on a space control register value and a time control register value.

12. The method of claim 11 wherein the space control register indicates a selected stream of data from a plurality of streams of data.

13. The method of claim 12, wherein the space control register is programmable.

14. The method of claim 11, wherein the time control register indicates one or more bits from a selected stream of data.

15. The method of claim 14, wherein the time control register is programmable.